I/O Products

IC697VAL134/IC697VAL132

GFK-2104
814-000438-000
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Isolated Scanning 12-bit 31-Channel Analog-to-Digital Converter Board (6U) with Built-in-Test and Screw Terminal interface

Features

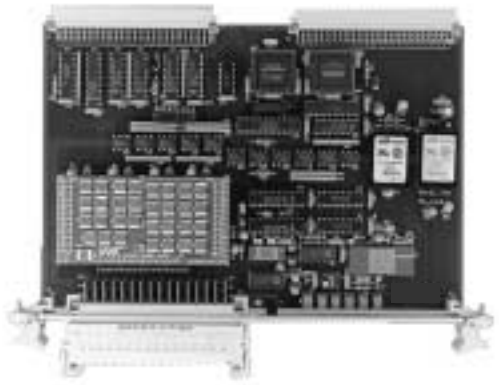
- Thirty one single-ended or 16 differential inputs
- Autoscanning; continuously digitizes inputs and stores results in dual-ported data registers
- Input ranges from ±50mV to ±10V
- Jumper-programmable gains of x1, x10, x100
- Selectable A/D ranges of ±5V, ±10V, 0 to +10V
- Aggregate conversion rate of 40kHz
- Supports real time Built-in-Test
- Input connector compatible with discrete wire cables
- Selectable data coding; offset binary or two's complement
- Overvoltage protected inputs
- Low pass input filters: 40Hz (IC697VAL134)
- Pull-down resistors prevent floating inputs
- Channel-to-bus isolation to 1,500V
- Accepts pluggable barrier strip cable connector with user screw interface
  - Connectors are latchable
  - Connectors are provided

Applications

- Instrumentation
- Process control
- Data acquisition
- Voltage measurement
- Factory automation

Table 1. Related Products

IC697VAL134	Analog Input, ±50mV to ±10V, 31 single-ended or 16 differential channels, 12-bit , 40Hz filter
IC697VAL132	Analog Input, 0 to 20mA, 31 single-ended or 16 differential channels, 12-bit



Introduction

The Analog-to-Digital Converter Board (ADC) provides isolated 12-bit analog-to-digital conversion for 31 single-ended analog input channels (16 differential) on 6U Eurocard for the VMEbus.

Selectable gain and A/D ranges support input voltage ranges from ±50mV to ±10V. To minimize system software overhead, all inputs are scanned and digitized continuously at an aggregate sample rate of 40,000 channels per second. Measurement data for each channel is constantly available to the VMEbus through a dual-ported Data Register. The 40Hz low pass input filters minimize the effects of system noise.

A jumper-selectable Programmable-Gain Amplifier (PGA) supports in-line voltage gains of x1, x10, or x100 for all channels. Full-scale ranges for the A/D Converter are selectable as ±5V, ±10V, or 0 to +10V. Data coding is software selectable as either offset binary or two's complement.

Inputs can be jumper configured as 16 differential channels, or 31 single-ended channels. A single front panel 32-pin DIN connector provides the user with 32 screw contacts to interface all input channels.

Figure 1 illustrates the internal functional organization of the ADC board.

Operating Mode

All 31 or 16 input channels are scanned continuously at the maximum sampling rate, and the resulting data is stored in dual-ported Data Registers for VMEbus access. Scanning starts automatically after any reset operation, and no other programming is required to start the A/D conversion process.

Built-in-Test Function (BIT)

Operation of the PGA, ADC, and associated control logic can be verified by selecting the BIT operating mode. In this mode, an internal reference voltage is applied to the input of the PGA, bypassing the analog input multiplexer. All data channels read through the control interface will reflect the selected BIT reference voltage.

Functional Characteristics

VMEbus Compliance: This product complies with VMEbus specification ANSI/IEEE ST 1014-1987 IEC821 and 297 with the following mnemonics:

A16:D16/D08 (EO) DTB Slave: 6U form factor

Board Address: The physical address is selected by on-board address jumpers, using VMEbus address lines A07 through A15. The ADC board occupies 128 bytes of address space, and can be located on any 64-word boundary in the Short I/O (A16) space.

Address Modifiers: Address modifier bits are jumper selected and decoded to respond to Nonprivileged Short I/O access, Supervisory Short I/O access, or to both access privileges.

System Reset: A System Reset establishes the following board status:
Automatic scanning of all channels
Front panel diagnostic LED indicator ON
Offset Binary Data Format

Front Panel System Diagnostic LED: A software-controlled front panel LED turns ON at System Reset, and can be turned OFF under software control to provide an external indication that Built-in-Test has been completed.

Analog Input Data Format: Analog inputs are digitized and stored in 32 dual-ported Data Registers (16 registers for differential operation) as 12-bit right-justified digital values.

Software-selectable data codes are Offset Binary and Two's Complement. In Two's Complement coding, the sign bit (D11) is extended through the most significant bits of the Data Register (D12 through D15).

Specifications

(At +25°C and rated power supplies unless otherwise noted.)

Input Characteristics

Number of Channels: 31 single-ended or 16 differential input channels

Voltage Ranges: ±50mV to ±10V, bipolar: or 0 to +100mV, 0 to +10V unipolar. Factory configured for ±10V input range.

Current Termination: 250Ω 0.01%
500Ω 0.01%

Current Ranges: 0 to 20mA, 4 to 20mA, +5 to 25mA

Input Impedance: 10MΩ minimum, line-to-line and line-to-common

Common-Mode Voltage (CMV): ±11V, maximum CMV for differential inputs; zero input signal. CMV is referenced to an analog ground common to all inputs.

Common-Mode Rejection Ratio (CMRR): Minimum CMRR for differential inputs; 350Ω source unbalance, DC-60Hz:

x100: 90dB
x10: 90dB
x1: 72dB

Input-to-VMEbus Isolation: 1,500VDC

Input Noise: Maximum noise referred to input, 10 to 1,000Hz, at $3\sigma^4$:

x100: 300Vpp
x10: 1.0mVpp
x1: 4.0mVpp

Bandwidth, Each Input: DC-to-Fc, where Fc is 40Hz for the 40Hz filter.

Input Filter: Single-pole passive low pass filter: -3dB at 40Hz ±20%

Overvoltage Protection: ±40V maximum sustained, power applied; ±25V power removed; ±40V transient for one second

Grounding: A user-configurable jumper connects the low input of channel 31 to an isolated ground reference.

Transfer Characteristics

Measurement Resolution: 12 bits (2^{-12})

Channel Scan Rate: 40kSPS (Kilosamples per second) minimum aggregate rate

Transfer Function:

Where:

$$E_{IN} = E_{LO} + E_{FSR} \times \frac{N_{ADC}}{4{,}096}$$

E_{IN} = Input voltage
E_{FSR} = Full-scale input range
E_{LO} = Lower end of input range
N_{ADC} = A/D Converter reading

Example:
For an N_{ADC} value of 0B33 HEX (2,867 decimal) in the ±5V range:
E_{IN} = -5.000 + [10.000 x (2,867/4,096)]; = +2.000V

A/D Converter Input Range: ±5V, ±10V, 0 to +10V; jumper selectable

A/D Converter Input Gain: x1, x10, x100, ±0.3%, jumper selectable

Accuracy:

Maximum Error:
Voltage Input = ±0.04% reading ±0.03% range ±2.0mV

Example:
For a +2.000V reading in the ±5V range:
Maximum Error = ±0.8mV ±3.0 mV ±2.0mV = ±5.8mV

Stability:
Temperature Drift, per °C =
±30PPM Reading ±25PPM Range ±20mV
Long-Term Drift, per 1,000 hr =
±50PPM Reading ±45PPM Range ±100µV

Interchannel Crosstalk:
-67dB maximum, DC to 1kHz with 40Hz filter

BIT Reference Voltage: Software selectable as 0.000V, +4.980V, +0.4928V and 9.91mV

BIT Reference Accuracy: ±30mV ±30PPM per °C

Physical/Environmental

Power Supply Requirements: +5VDC (±5%) at 2.5A maximum

Temperature: 0 to +65°C, operating
-40 to +85°C, storage

Humidity: 20 to 80% relative, noncondensing

Altitude: Operation to 3,000m

Cooling: Forced air convection (standard VME slot)

Dimensions: Dual height Eurocard (6U) board

Weight: 0.7kgm maximum

Input Connector (P3): 32-pin DIN 41 612, VG and IEC connectors. Connectors interface with 22 to 14AWG wire utilizing binding screw terminals and connector latches.

MTBF: 139,800 hours (MIL STD 217F)

Agency Approvals: UL1604 with C-UL

Certification by Underwriters Laboratory for use in Class 1, Div. 2, Groups A, B, C, D Hazardous Locations. Board complies with applicable CSA Standards as evaluated by UL. The C-UL mark is accepted throughout Canada.

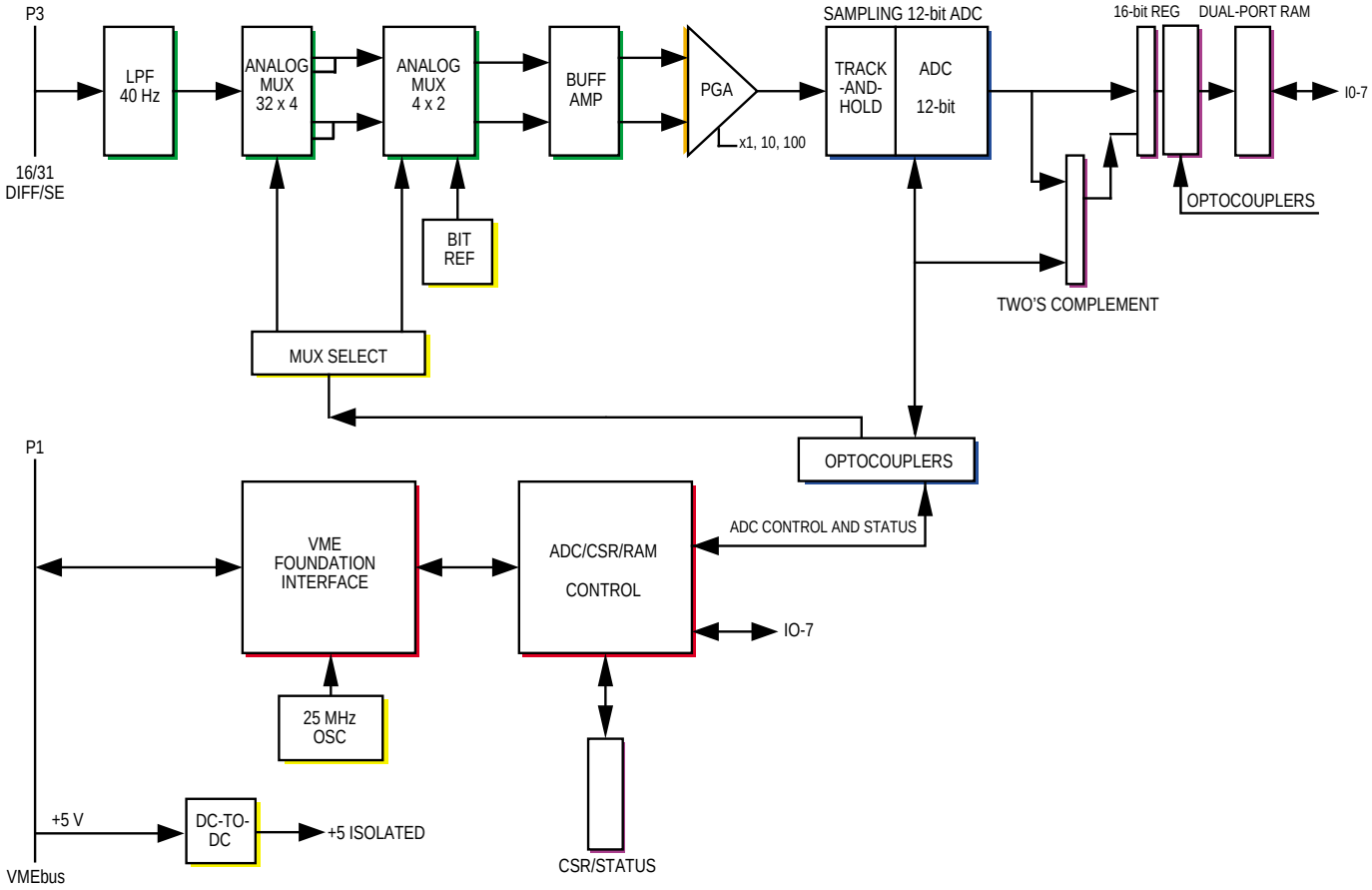


Figure 1. Functional Block Diagram